REMARKS

Applicant hereby traverses the current rejections and requests reconsideration and withdrawal of such in light of the remarks contained herein. Claims 1-28 are pending in this application.

Rejection under 35 U.S.C. § 102(e)

Claims 1-3, 8-13, 16-21, and 24-27 are rejected under 35 U.S.C. § 102(e) as being anticipated by United States Patent No. 6,694,492 to Shakkarwar (hereinafter "Shakkarwar").

The Applicant respectfully asserts however, that the Current Action's rejection of these claims cannot meet the requirement of an anticipation rejection. It is well settled that "anticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, arranged as in the claim." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984); *citing Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983) (emphasis added). The Applicant asserts that each of claims 1-3, 8-13, 16-21, and 24-27 recite limitations not taught by Shakkarwar.

Claim 1 requires "an embedded micro-controller constructed on the VLSI die,... adapted to monitor and control the VLSI environment to optimize the integrated circuit operation." The Current Action points to several citations in an attempt to meet this claim limitation (*see* Current Action pg. 2); however, the Applicant respectfully submits that Shakkarwar fails to teach this claim limitation. Instead, Shakkarwar merely describes "a power controller 108 coupled to a CPU 102 and the voltage regulator module 109" that can only "provide a voltage control signal 120 to voltage regulator module 109 and an operating rate control signal 118 to clock register 104." (*see* Shakkarwar col. 5, lines 44-55). The Applicant respectfully submits, however, that reference to figure 1 of Shakkarwar makes clear that power controller 108 is not constructed on the die. Shakkarwar further describes "a test controller 110 that may be coupled to central processing unit 102 and voltage regulator module 109" that merely "provides a operating rate control signal 126 to clock register 104 or a value 127 to one-time programmable clock register 103" or "provides an operating voltage control signal 125 to voltage regulator module 109." Again, the Applicant respectfully

submits that reference to figure 1 of Shakkarwar makes clear that power controller 110 is not constructed on the die. Finally, Shakkarwar discloses an "internal controller 130" that can only "receive an output 138 from thermal sensor 107, an input 145 from battery status indicator 148, and an input 146 from user-programmable register 137." Internal controller 130 "may apply test vectors 131 controlled by a diagnostic program to central processing unit core 106." (*see* Shakkarwar col. 6, lines 40-50). The Applicant respectfully points out that "receiving" and "applying test vectors" is not the same as monitoring the VLSI environment. Moreover, the Applicant believes such limitation is not inherent within the disclosure of Shakkarwar as there is no discussion that controller 130 monitors the information it receives; also, there is no discussed relationship between the "receiving" and "applying test vectors." Therefore, Shakkarwar fails to teach "an embedded micro-controller constructed on the VLSI die...adapted to monitor and control the VLSI environment...," and instead discloses only controllers that are not constructed on the die and a controller that does not monitor the VLSI environment. Therefore, the Applicant respectfully requests the Examiner withdraw the 35 U.S.C. § 102(e) rejection of record.

Claim 8 requires monitoring and controlling a VLSI environment of the integrated circuit with [an] embedded micro-controller. The Current Action points to several citations in an attempt to meet this claim limitation (*see* Current Action pg. 2); however, the Applicant respectfully submits that Shakkarwar fails to teach this claim limitation. Instead, Shakkarwar merely describes "a power controller 108 coupled to a CPU 102 and the voltage regulator module 109" that can only "provide a voltage control signal 120 to voltage regulator module 109 and an operating rate control signal 118 to clock register 104." (*see* Shakkarwar col. 5, lines 44-55). The Applicant respectfully submits, however, that reference to figure 1 of Shakkarwar makes clear that power controller 108 is not constructed on the die. Shakkarwar further describes "a test controller 110 that may be coupled to central processing unit 102 and voltage regulator module 109" that merely "provides a operating rate control signal 126 to clock register 104 or a value 127 to one-time programmable clock register 103" or "provides an operating voltage control signal 125 to voltage regulator module 109." Again, the Applicant respectfully submits that reference to figure 1 of Shakkarwar makes clear that power controller 110 is not constructed on the die. Finally, Shakkarwar discloses an "internal controller 130" that can only "receive an output 138 from thermal sensor 107, an input 145 from battery status indicator 148, and an input 146 from user-programmable register 137."

Internal controller 130 "may apply test vectors 131 controlled by a diagnostic program to central processing unit core 106." (*see* Shakkarwar col. 6, lines 40-50). The Applicant respectfully points out that "receiving" and "applying test vectors" is not the same as monitoring the VLSI environment. Moreover, the Applicant believes such limitation is not inherent within the disclosure of Shakkarwar as there is no discussion that controller 130 monitors the information it receives; also, there is no discussed relationship between the "receiving" and "applying test vectors." Therefore, Shakkarwar fails to teach "an embedded micro-controller constructed on the VLSI die...adapted to monitor and control the VLSI environment...," and instead discloses only controllers that are not constructed on the die and a controller that does not monitor the VLSI environment. Therefore, the Applicant respectfully requests the Examiner withdraw the 35 U.S.C. § 102(e) rejection of record.

Claim 16 requires " code for controlling an embedded micro-controller..., wherein the micro-controller monitors and controls a VLSI environment of the processor." The Current Action points to several citations in an attempt to meet this claim limitation (*see* Current Action pg. 2); however, the Applicant respectfully submits that Shakkarwar fails to teach this claim limitation. Instead, Shakkarwar merely describes "a power controller 108 coupled to a CPU 102 and the voltage regulator module 109" that can only "provide a voltage control signal 120 to voltage regulator module 109 and an operating rate control signal 118 to clock register 104." (*see* Shakkarwar col. 5, lines 44-55). The Applicant respectfully submits, however, that reference to figure 1 of Shakkarwar makes clear that power controller 108 is not constructed on the die. Shakkarwar further describes "a test controller 110 that may be coupled to central processing unit 102 and voltage regulator module 109" that merely "provides a operating rate control signal 126 to clock register 104 or a value 127 to one-time programmable clock register 103" or "provides an operating voltage control signal 125 to voltage regulator module 109." Again, the Applicant respectfully submits that reference to figure 1 of Shakkarwar makes clear that power controller 110 is not constructed on the die. Finally, Shakkarwar discloses an "internal controller 130" that can only "receive an output 138 from thermal sensor 107, an input 145 from battery status indicator 148, and an input 146 from user-programmable register 137." Internal controller 130 "may apply test vectors 131 controlled by a diagnostic program to central processing unit core 106." (*see* Shakkarwar col. 6, lines 40-50). The Applicant respectfully points out that "receiving" and "applying test vectors" is not the same as monitoring the VLSI environment. Moreover, the Applicant

believes such limitation is not inherent within the disclosure of Shakkarwar as there is no discussion that controller 130 monitors the information it receives; also, there is no discussed relationship between the "receiving" and "applying test vectors." Therefore, Shakkarwar fails to teach "an embedded micro-controller constructed on the VLSI die...adapted to monitor and control the VLSI environment...," and instead discloses only controllers that are not constructed on the die and a controller that does not monitor the VLSI environment. Therefore, the Applicant respectfully requests the Examiner withdraw the 35 U.S.C. § 102(e) rejection of record.

Claim 24 requires "means for monitoring and controlling a VLSI environment of the integrated circuit with the embedded micro-controller." The Current Action points to several citations in an attempt to meet this claim limitation (*see* Current Action pg. 2); however, the Applicant respectfully submits that Shakkarwar fails to teach this claim limitation. Instead, Shakkarwar merely describes "a power controller 108 coupled to a CPU 102 and the voltage regulator module 109" that can only "provide a voltage control signal 120 to voltage regulator module 109 and an operating rate control signal 118 to clock register 104." (*see* Shakkarwar col. 5, lines 44-55). The Applicant respectfully submits, however, that reference to figure 1 of Shakkarwar makes clear that power controller 108 is not constructed on the die. Shakkarwar further describes "a test controller 110 that may be coupled to central processing unit 102 and voltage regulator module 109" that merely "provides a operating rate control signal 126 to clock register 104 or a value 127 to one-time programmable clock register 103" or "provides an operating voltage control signal 125 to voltage regulator module 109." Again, the Applicant respectfully submits that reference to figure 1 of Shakkarwar makes clear that power controller 110 is not constructed on the die. Finally, Shakkarwar discloses an "internal controller 130" that can only "receive an output 138 from thermal sensor 107, an input 145 from battery status indicator 148, and an input 146 from user-programmable register 137." Internal controller 130 "may apply test vectors 131 controlled by a diagnostic program to central processing unit core 106." (*see* Shakkarwar col. 6, lines 40-50). The Applicant respectfully points out that "receiving" and "applying test vectors" is not the same as monitoring the VLSI environment. Moreover, the Applicant believes such limitation is not inherent within the disclosure of Shakkarwar as there is no discussion that controller 130 monitors the information it receives; also, there is no discussed relationship between the "receiving" and "applying test vectors." Therefore, Shakkarwar fails to teach "an embedded

micro-controller constructed on the VLSI die...adapted to monitor and control the VLSI environment...," and instead discloses only controllers that are not constructed on the die and a controller that does not monitor the VLSI environment. Therefore, the Applicant respectfully requests the Examiner withdraw the 35 U.S.C. § 102(e) rejection of record.

Claims 2-3, 9-13, 17-21, and 25-27 depend from their respective base claims, and thus inherit all the limitations of the claims from which they depend. Additionally, each of claims 2-3, 9-13, 17-21, and 25-27 further set forth limitations not taught or suggested by Shakkarwar. The Applicant respectfully assert that claims 2-3, 9-13, 17-21, and 25-27 are allowable at least for the reasons set forth above with respect to claims 1, 8, 16, and 24. Therefore, the Applicant respectfully requests the Examiner withdraw the 35 U.S.C. § 102(e) rejection of record.

Rejection under 35 U.S.C. § 103(a)

Claims 4, 14, 22, and 28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shakkarwar in view of U.S. Patent Application Publication 2003/0225999 to Rogenmoser (hereinafter "Rogenmoser").

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one or ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references must teach or suggest all the claim limitations. *See* M.P.E.P. § 2143; *In re Vaeck*, 947 F.2d 488, 20 USPQ 2d 1438 (Fed. Cir. 1991). Without conceding the first or second criteria, the Applicant respectfully submits that the Current Action does not establish a prima facie case because the proposed combination fails to teach or suggest all of the limitations of the rejected claims.

The Applicant respectfully points out that the combination of Shakkarwar and Rogenmoser fails to teach or suggest all of the claim limitations of Applicant's invention. In the Current Action, the Examiner remarks "Shakkarwar does not disclose the IC having two or more processor cores each with an integer and floating point unit and temperature sensors at each of the units." The Current Action then states "it would have been obvious to combine

Shakkarwar and Rogenmoser because applying Shakkarwar's monitoring of temperature at each unit and transferring a processing workload...would maintain a processor such as Rogenmoser's to within design limits for overheating which would meet restrictions for export." (*see* Current Action, pg. 3). However, as discussed above, claims 4, 14, 22, and 28 depend from their respective base claims, and thus require an embedded micro-controller monitoring and controlling a VLSI environment. As discussed above, Shakkarwar fails to teach an embedded micro-controller constructed on the die monitoring and controlling a VLSI environment, and instead discloses only controllers that are not constructed on the die and a controller that does not monitor the VLSI environment. Further, Rogenmoser is not relied upon to teach the missing limitation. Even if the Examiner's remarks are correct, which the Applicant does not concede they are, the combination of Shakkarwar and Rogenmoser fails to teach or suggest every claim limitation of Applicant's invention. Thus, the Applicant respectfully asserts that claims 4, 14, 22, and 28 are patentable over the 35 U.S.C. § 103(a) rejection of record.

Claims 5, 15, and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shakkarwar in view of Korean Patent Publication 9405466 B1 to Kim (hereinafter "Kim").

The Applicant respectfully submits that the Current Action does not establish a prima facie case of obviousness because the combination of Shakkarwar and Kim fails to teach or suggest all of the limitations of the rejected claims. In the Current Action, the Examiner remarks "Shakkarwar does not specifically disclose ammeter comprising VCO's. Kim discloses ammeters comprising VCO's. The Current Action then states "it would have been obvious to combine Shakkarwar and Kim because monitoring current levels with ammeters and VCO's would provide Shakkarwar's system with a way of determining current...to determine over-temperature due to current levels." (*see* Current Action, pg. 4). However, as discussed above, claims 5, 15, and 23 depend from their respective base claims, and thus require an embedded micro-controller monitoring and controlling a VLSI environment. As discussed above, Shakkarwar fails to teach an embedded micro-controller constructed on the die monitoring and controlling a VLSI environment, and instead discloses only controllers that are not constructed on the die and a controller that does not monitor the VLSI environment. Further, Kim is not relied upon to teach the missing limitation. Even if the Examiner's remarks are correct, which the Applicant does not concede they are, the

combination of Shakkarwar and Kim fails to teach or suggest every claim limitation of Applicant's invention. Thus, the Applicant respectfully asserts that claims 5, 15, and 23 are patentable over the 35 U.S.C. § 103(a) rejection of record.

In view of the above amendment, applicant believes the pending application is in condition for allowance. Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 08-2025, under Order No. 200208727-1 from which the undersigned is authorized to draw.

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail, Label No. EV629198558 in an envelope addressed to: M/S Amendment, Commissioner for Patents, Alexandria, VA 22313.

Date of Deposit: 07/20/2005

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